Justin T. Wilford

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EDUCATION

Master of Science, Computer Engineering **Aug 2022**
Bachelor of Science, Computer Engineering and Computer Science **May 2021**
Viterbi School of Engineering **GPA: 3.61**
University of Southern California – Los Angeles, CA
Related Coursework:

- MOS VLSI Circuit Design
- Intro to System on Chip
- Intro to Digital Circuit Design
- Intro to Operating Systems
- Intro to Algorithms and Theory of Computing
- Computer Systems Organization
- Intro to Embedded Systems
- Intro to the Internet of Things
- Intro to Internetworking

SKILLS

Software: Python, C++, C, Java, C#, Verilog, Xilinx ISE, Cadence Virtuoso, QuestaSim
Hardware: FPGA, RTL Design, Transistor-Level Design/Layout, Arduino, Raspberry Pi
Other Computing: Linux, Windows, Git, GDB

EXPERIENCE

Student Software Developer **October 2017 - Present**
University of Southern California: Information Technology Services – Los Angeles, CA

- Full-Stack developer for web-based applications
- Lead a team of 3 to 4 student developers to implement projects using the MEAN stack with Docker Swarm and Jenkins for deployment
- Designed a robust RESTful API utilizing a microservice architecture

Web Developer – Viterbi Conversations in Ethics **September 2019 – Present**
USC Viterbi School of Engineering: Engineering Writing Program – Los Angeles, CA

- Design and maintain an online magazine (https://vce.usc.edu/)
- Student-run publication emphasizing ethics in engineering fields
- Website utilizes WordPress with custom plugins and widgets

PROJECTS

Pong for FPGA – More details at http://jwilford.me/projects/pong-for-fpga/

- Collaborated with another student to develop a Pong clone on an FPGA
- Created a simple and modular video game engine using Verilog and Xilinx ISE, with the intent to repurpose for other games
- Utilized a state machine to handle different functions of the game engine, such as collision detection, player movement, and VGA output
- Implemented and demonstrated the game running on a Diligent Nexys 3 FPGA

10-bit Multiply-Accumulator Schematic and Layout – More details at http://jwilford.me/projects/10-bit-mac/

- Designed a 10-bit Multiply-Accumulator at the transistor level
- Utilized Cadence Virtuoso for both schematic and layout
- Incorporated transistor sizing to maintain setup and hold times, and to decrease overall delays
- Created a test bench to verify all functionality of the design